CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-35. (Cancelled)

36. (Currently Amended) A method comprising:

during compaction of a circuit layout, determining at a computer device a first direction associated with [[a]]the circuit layout;

selecting at the computer device a first portion of a first transistor in response to determining the first portion extends outward in the first direction from a first logical device of the circuit layout, the first logical device comprising the first transistor;

in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction;

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device;

determining at the computer device a second direction associated with the circuit layout, the second direction different from the first direction;

selecting at the computer device a third portion of a second transistor of the circuit layout in response to determining the third portion extends outward in the second direction from a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the second direction;

reshaping at the computer device a fourth portion of the second logical device in response to reducing the size of the second logical device.

37. (Previously Presented) The method of claim 36, wherein the first portion of the first transistor comprises a first transistor finger.

38. (Previously Presented) The method of claim 37, wherein the second portion of the first logical device comprises a second transistor finger of the first transistor.

39. (Previously Presented) The method of claim 37, wherein the second portion of the first logical device comprises a transistor finger of a second transistor.

40. (Previously Presented) The method of claim 37, wherein reshaping the first portion comprises reducing a size of the first transistor finger.

41. (Previously Presented) The method of claim 37, wherein reshaping the first portion comprises removing the first transistor finger.

42. (Previously Presented) The method of claim 36, wherein reshaping the first portion comprises rotating the first transistor.

43. (Previously Presented) The method of claim 36, further comprising reshaping a third portion of the first logical device in response to reducing the size of the first transistor portion.

44. (Previously Presented) The method of claim 36, further comprising:

storing a first state associated with the circuit layout at the computer device in response to selecting the first portion of the first transistor;

in response to reshaping the first portion of the first transistor, determining if a size of the circuit layout has been reduced; and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state.

45. (Previously Presented) The method of claim 44, wherein determining if the size of the circuit layout has been reduced comprises determining if the size of the circuit layout has been reduced in the first direction.

46. (Previously Presented) The method of claim 36, further comprising

selecting at the computer device a third portion of a second transistor of the circuit layout in response to determining the third portion extends outward in the first direction from a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the third portion, reshaping at the computer device the third portion of the second transistor to reduce a size of the second logical device in the first direction;

reshaping at the computer device a fourth portion of the second logical device in response to reducing the size of the second logical device.

47- 70. (Cancelled)

71. (Previously Presented) The method of claim 44, wherein the third portion of the second transistor comprises a first transistor finger.

72. (Previously Presented) The method of claim 71, wherein the fourth portion of comprises a second transistor finger of the second transistor.

73. (Previously Presented) The method of claim 71, wherein the fourth portion comprises a transistor finger of a third transistor.

74. (Previously Presented) The method of claim 71, wherein reshaping the third portion comprises reducing a size of the first transistor finger.

75. (Previously Presented) The method of claim 71, wherein reshaping the third portion comprises removing the first transistor finger.

76. (Previously Presented) The method of claim 71, wherein reshaping the third portion comprises rotating the first transistor.

77. (Previously Presented) The method of claim 47, wherein the third portion of the second transistor comprises a first transistor finger.

78. (Previously Presented) The method of claim 77, wherein reshaping the third portion comprises reducing a size of the first transistor finger.

79. (New) A method comprising:

during compaction of a circuit layout, determining at a computer device a first direction associated with the circuit layout;

selecting at the computer device a first portion of a first transistor in response to determining the first portion extends outward in the first direction from a first logical device of the circuit layout, the first logical device comprising the first transistor;

in response to selecting the first portion, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction;

reshaping at the computer device a second portion of the first logical device in response to reducing the size of the first logical device.